IN THE CLAIMS:

Claims 1-31 (Canceled)

Claim 32 (New) A non-volatile semiconductor memory device comprising:

a non-volatile memory cell; and

a write circuit, configured to write data in said memory cell, thereby causing an alteration in a write state of said memory cell, for changing the supply of said write control voltage in order to slow down the alteration, and for terminating the alteration amid slowing down the alteration.

Claim 33 (New) The device according to claim 32, wherein the write voltage is stepwise increased.

Claim 34 (New) The device according to claim 32, wherein the write circuit determines if the write state has reached a first level, and changes the supply of the write control voltage in response to an advent of the first level.

Claim 35 (New) The device according to claim 34, wherein the write circuit determines if the write state has reached a second level, and terminates the alteration in response to an advent of the second level.

Claim 36 (New) The device according to claim 32, further comprising a word line connected to the memory cell at its gate electrode to which the write voltage is applied, and a bit line coupled to the memory cell at its drain electrode to which the write control voltage is applied.

Claim 37 (New) The device according to claim 32, wherein the write circuit is capable of writing data more than one bit in the memory cell.

Claim 38 (New) A non-volatile semiconductor memory device comprising:

a non-volatile memory cell; and

a write circuit, configured to write data in said memory cell, for applying a read voltage to said memory cell in order to read out data stored in said memory cell, for applying a first verify voltage to said memory cell in order to determine if a write state of said memory cell has reached a first level, for applying a write voltage and a write control voltage having a first effective voltage level to said memory cell, if the write state has not reached the first level, for applying the write voltage and the write control voltage having a second effective voltage level to said memory cell, if the write state has reached the first level, for applying a second verify voltage to said memory cell in order to determine if the write state of said memory cell has reached a second level, and for applying the write voltage and the write control voltage having a third effective voltage level to said memory cell in order to terminate a writing data in said memory cell, if the write state has reached the second level,

wherein a difference between the read voltage and the second verify voltage is larger than a difference between the first verify voltage and the second verify voltage.

Claim 39 (New) The device according to claim 38, wherein the write voltage is stepwise increased.

Claim 40 (New) The device according to claim 38, further comprising a word line connected to the memory cell at its gate electrode to which the write voltage is applied, and a bit line coupled to the memory cell at its drain electrode to which the write control voltage is applied.

Claim 41 (New) The device according to claim 38, wherein the write circuit is capable of writing data more than one bit in the memory cell.